CLAIMS

WHAT IS CLAIMED IS:

1. An input processing device for use in a re-multiplexing module that processes input packet data, comprising:

an input interface that receives the input packet data;

an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer; and

a packet identifier table coupled to the input processor.

2. The input processing device of claim 1, wherein the input processor includes a serial-to-parallel converter for converting the input packet data received from the input interface.

3. The input processing device of claim 1, wherein the input processor includes a input processor control logic portion that validates the input packet data.

4. The input processing device of claim 3, wherein the input processor control logic validates the input packet data by extracting a packet identifier number from a header in the input packet data and checking the packet identifier number with the packet identifier table.

5. The input processing device of claim 1, wherein the input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field.

6. The input processing device of claim 1, wherein the input processor includes a data delay register that delays the input packet data before the input processor writes data to the packet buffer.

7. The input processing device of claim 1, wherein the input processor includes a time reference generator that generates timestamp values for the input packet data.

8. The input processing device of claim 1, wherein the input processor includes a host processor interface.

9. The input processing device of claim 1, wherein the input processor is a field programmable gate array.

10. The input processing device of claim 1, wherein the packet identifier table is divided into an active table containing values used by the input processor to select packets for storage in a input packet data stream and a pending table containing values that can be modified by the host processor while the active table is being used by the active table.

11. An input processing device for use in a re-multiplexing module that processes input packet data, comprising:

an input interface that receives the input packet data;

an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer, the input processor including

a serial-to-parallel converter for converting the input packet data received from the input interface;

an input processor control logic portion that receives data from the serial-to-parallel converter;

a program clock reference detector that checks the input packet data for a valid program clock reference field;

a data delay register that delays the input packet data before the input processor writes data to the packet buffer;

a time reference generator that generates timestamp values for the input packet data; and

a host processor interface; and

a packet identifier table coupled to the input processor.

12. The input processing device of claim 11, wherein the input processor is a field programmable gate array.

13. The input processing device of claim 11, wherein the packet identifier table is divided into an active table containing values used by the input processor to select packets for storage in a input packet data stream and a pending table containing values that can be modified by the host processor while the active table is being used by the active table.

14. The input processing device of claim 11, wherein the input packet data includes a plurality of packets, and wherein the input processor control logic portion validates the input packet data by extracting a packet identifier number from a header in a packet and checking the packet identifier number with the packet identifier table.

15. The input processing device of claim 11, wherein the input packet data includes a plurality of packets, and wherein the timestamp value generated by the time reference generator corresponds to a time period during which a packet passes through the re-multiplexing module.